

5 What is claimed is:

1. A semiconductor leadframe comprising:

a plate-type frame body having an opening at its center;

10 a chip paddle disposed centrally within the opening of said plate-type frame body;

a plurality of leads extending inwardly in a lengthwise direction from said plate-type frame body toward said opening, said plurality of leads being spaced at regular intervals about the perimeter of said chip paddle;

15 at least two tie bars extending inwardly from said plate-type frame body, said at least two tie bars connecting said chip paddle to said plate-type frame body; and wherein said plurality of leads are of at least two different lengths.

2. A semiconductor leadframe comprising:

a plate-type frame body having an opening at its center;

20 a chip paddle disposed centrally within said opening of said plate-type frame body, said chip paddle having a plurality of sides and corners;

a plurality of leads extending inwardly in a lengthwise direction from said plate-type frame body toward said opening, said plurality of leads being spaced at regular intervals about the perimeter of said chip paddle;

25 at least two tie bars extending inwardly from said plate-type frame body, said at least two tie bars connecting said chip paddle to said plate-type frame body; and

30 wherein said plurality of leads proximate each of said sides of said chip paddle include at least two outer leads and at least one inner lead, the outer leads being of a first length and the inner lead being of a second length, said first length and said second length being unequal.

3. The semiconductor leadframe of claim 2, wherein said plurality of leads having a first length are longer than said plurality of leads having a second length.

35 4. The semiconductor leadframe of claim 2, wherein said plurality of leads having a first length are shorter than said plurality of leads having a second length.

5           5. The semiconductor leadframe of claim 2, wherein said chip paddle is substantially rectangular.

10           6. The semiconductor leadframe of claim 2, wherein said corners of said chip paddle are chamfered.

15           7. The semiconductor leadframe of claim 2, wherein said leadframe is adapted for use in an MLF type semiconductor package.

20           8. A semiconductor package comprising:  
            a chip paddle, said chip paddle having an upper surface, a lower surface, a plurality of sides and corners;  
            a semiconductor chip, said semiconductor chip mounted on said upper surface of said chip paddle;  
            a plurality of leads in electrical communication with said semiconductor chip and being spaced at regular intervals about the perimeter of and apart from said chip paddle;  
            encapsulation material, said encapsulation material enclosing the semiconductor chip, the chip paddle and the plurality of leads and leaving only the lower surfaces of the chip paddle and the plurality of leads exposed; and  
25           wherein said plurality of leads are of at least two different lengths.

30           9. The semiconductor package of claim 8, wherein said plurality of leads proximate each of said sides of said chip paddle include at least two outer leads and at least one inner lead, the outer leads being of a first length and the inner lead being of a second length, said first length and said second length being unequal.

35           10. The semiconductor package of claim 9, wherein said plurality of leads having a first length are longer than said plurality of leads having a second length.

            11. The semiconductor package of claim 9, wherein said plurality of leads having a first length are shorter than said plurality of leads having a second length.

5           12. The semiconductor package of claim 8, wherein said chip paddle is substantially rectangular.

13. The semiconductor package of claim 8, wherein said corners of said chip paddle are chamfered.

10           14. The semiconductor package of claim 8, wherein the package is an MLF type semiconductor package.

15           15. A method of producing a packaged semiconductor, said method comprising the steps of:

15           providing a semiconductor leadframe having a plate-type frame body having an opening at its center, a chip paddle disposed centrally within the opening of said plate-type frame body, a plurality of leads extending inwardly in a lengthwise direction from said plate-type frame body toward said opening, said plurality of leads being spaced at regular intervals about the perimeter of said chip paddle, at least two tie bars extending inwardly from said plate-type frame body, said at least two tie bars connecting said chip paddle to said plate-type frame body, and wherein said plurality of leads are of at least two different lengths;

              mounting a semiconductor chip to an upper surface of the chip paddle;

              wiring the semiconductor chip to the plurality of leads;

25           encapsulating the semiconductor chip and the semiconductor leadframe within an encapsulation material, wherein lower surfaces of said chip paddle, said plurality of leads and said tie bars remain exposed; and

              singulating each of said at least two tie bars.

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